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Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>				<i>Complete if Known</i>		
				Application Number	10/720,562	
				Filing Date	11/24/2003	
				First Named Inventor	Correale, Jr. et al.	
				Art Unit	2925	
Examiner Name	GARBOWSKI					
Sheet	1	of	2	Attorney Docket Number	YOR920030359US1	

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
W		US- 5594368		USAMI	
		US- 5818256		USAMI	
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

Examiner Signature		Date Considered	10/18/03
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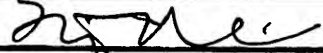
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Substitute for form 1449B/PTO		<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Application Number	10/720,562
		Filing Date	11/24/2003
		First Named Inventor	Correale, Jr. et al.
		Art Unit	2825
		Examiner Name	GARBOWSKI
Sheet 2 of 2	Attorney Docket Number	YOR920030359US1	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials <sup>a</sup>	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
W		LACKEY ET AL., Managing power and performance for System-on-Chip designs using Voltage Islands, Proceedings of the 2002 IEEE/ACM International conference on Computer-aided design, 11/11/2002, Page(s) 195-202	
W		USAMI ET AL., CLUSTERED VOLTAGE SCALING TECHNIQUES FOR LOW-POWER DESIGN, International Symposium on Low-Power Electronic Design, 4/1/1995, Page(s) 3-8, Publisher: ACM Press	
W		USAMI ET AL., AUTOMATED LOW-POWER TECHNIQUE EXPLOITING MULTIPLE SUPPLY VOLTAGES APPLIED TO A MEDIA PROCESSOR, IEEE Journal of Solid-State Circuits, 3/1/1998, Page(s) 463-472, Volume 33, Number 3	
W		YEH ET AL., LAYOUT TECHNIQUES SUPPORTING THE USE OF DUAL SUPPLY VOLTAGES FOR CELL-BASED DESIGNS, Proc. ACM/IEEE Design Auto. Conf., 6/1/1999, Page(s) 62-67	

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<sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>Applicant is to place a check mark here if English language Translation is attached.

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